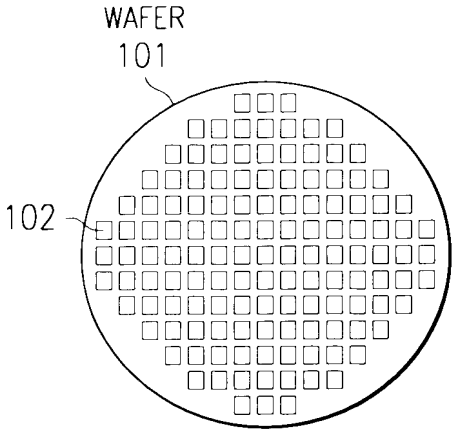


FIG. 1A

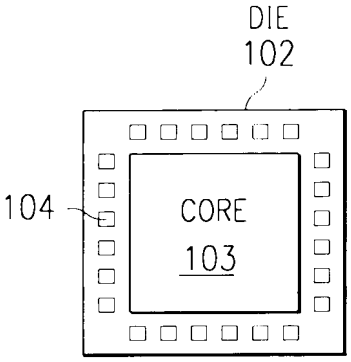


FIG. 1B

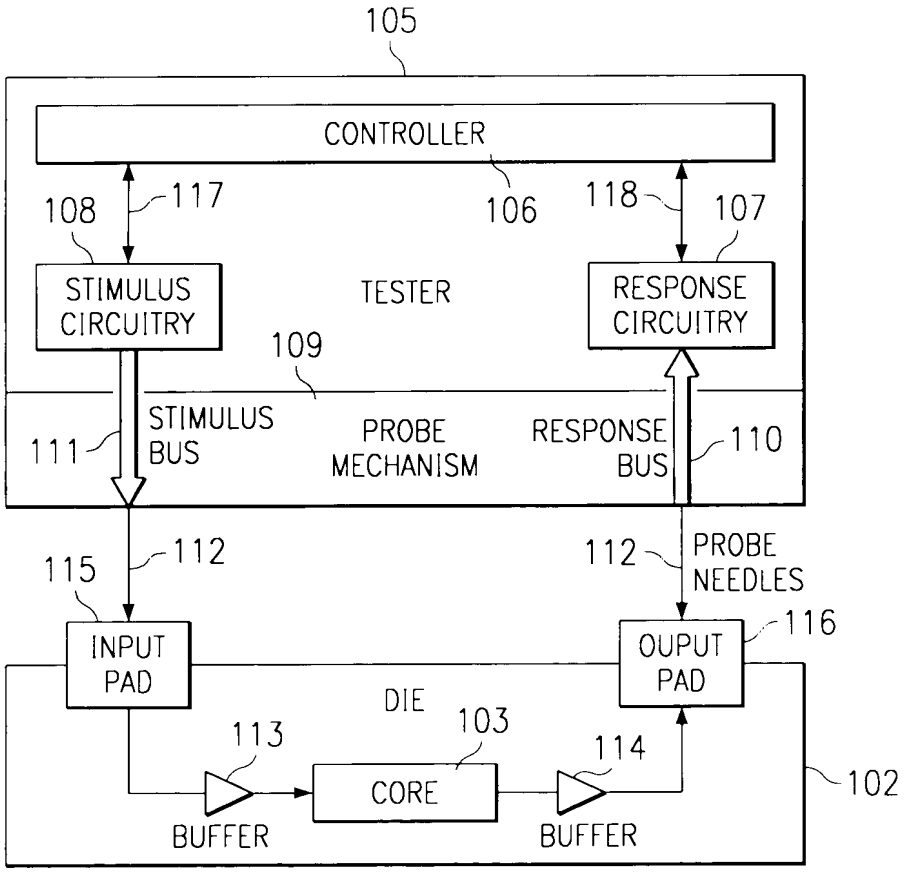


FIG. 1C

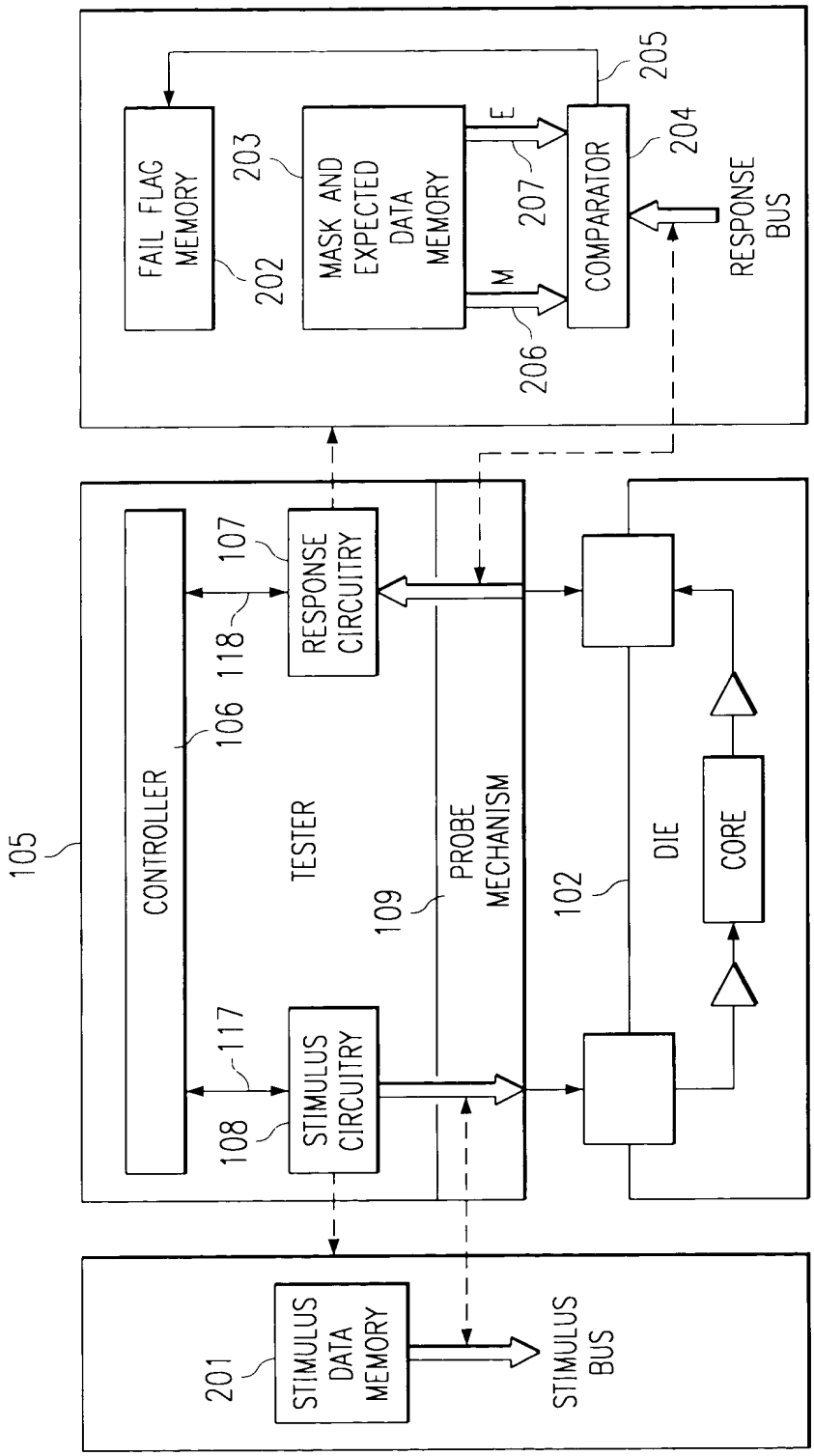

105
CONTROLLER
106
TESTER
RESPONSE CIRCUITRY
107
118
PROBE MECHANISM
109
STIMULUS CIRCUITRY
117
108
DIE
102
CORE
FAIL FLAG MEMORY
202
MASK AND EXPECTED DATA MEMORY
203
E
M
207
206
COMPARATOR
204
205
RESPONSE BUS
STIMULUS DATA MEMORY
201
STIMULUS BUS

FIG. 2

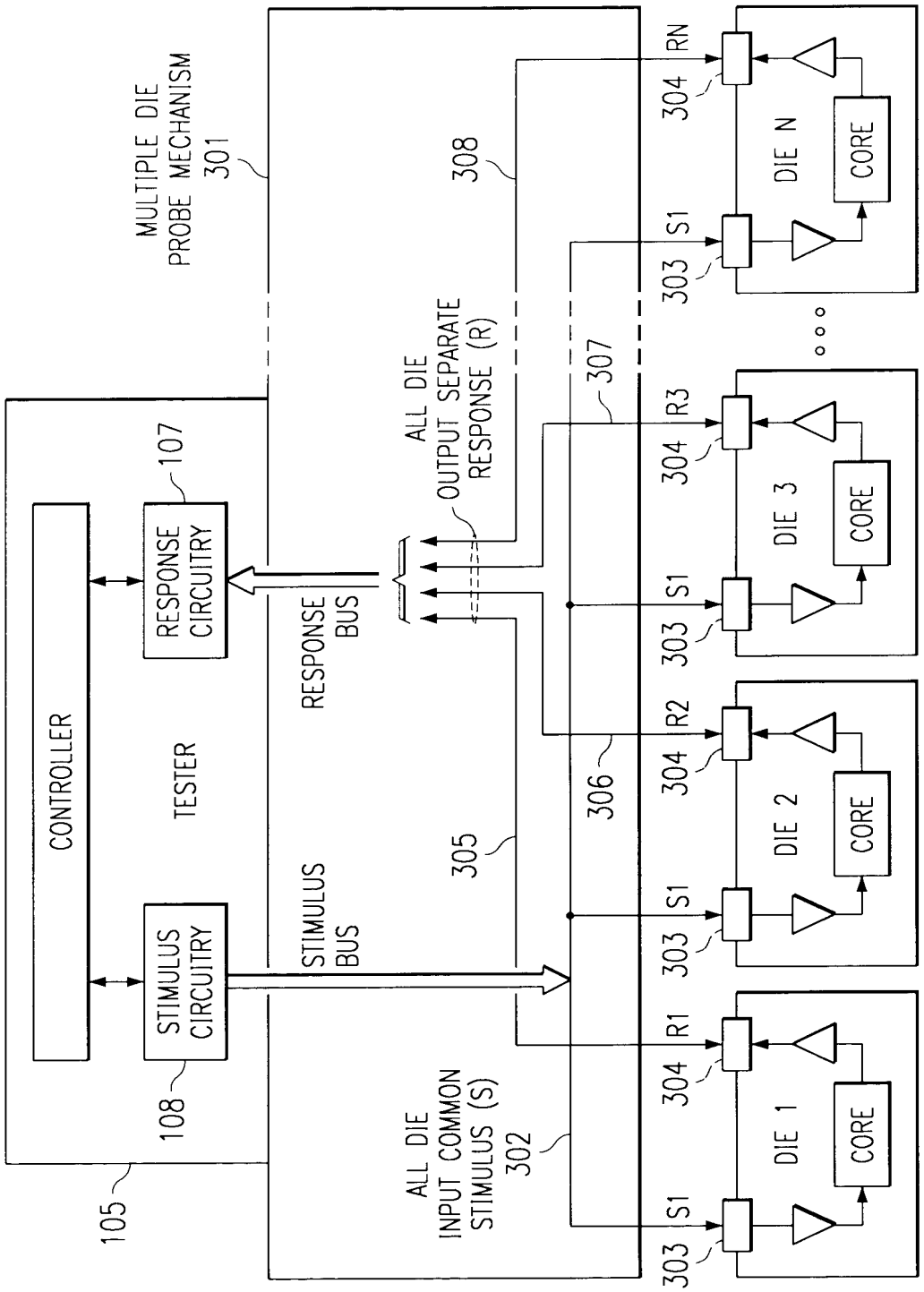

MULTIPLE DIE PROBE MECHANISM 301
CONTROLLER
TESTER
STIMULUS CIRCUITRY
RESPONSE CIRCUITRY
107
108
105
STIMULUS BUS
RESPONSE BUS
ALL DIE OUTPUT SEPARATE RESPONSE (R)
ALL DIE INPUT COMMON STIMULUS (S) 302
305
306
307
308
S1
R1
R2
R3
RN
303
304
DIE 1
DIE 2
DIE 3
DIE N
CORE

FIG. 3

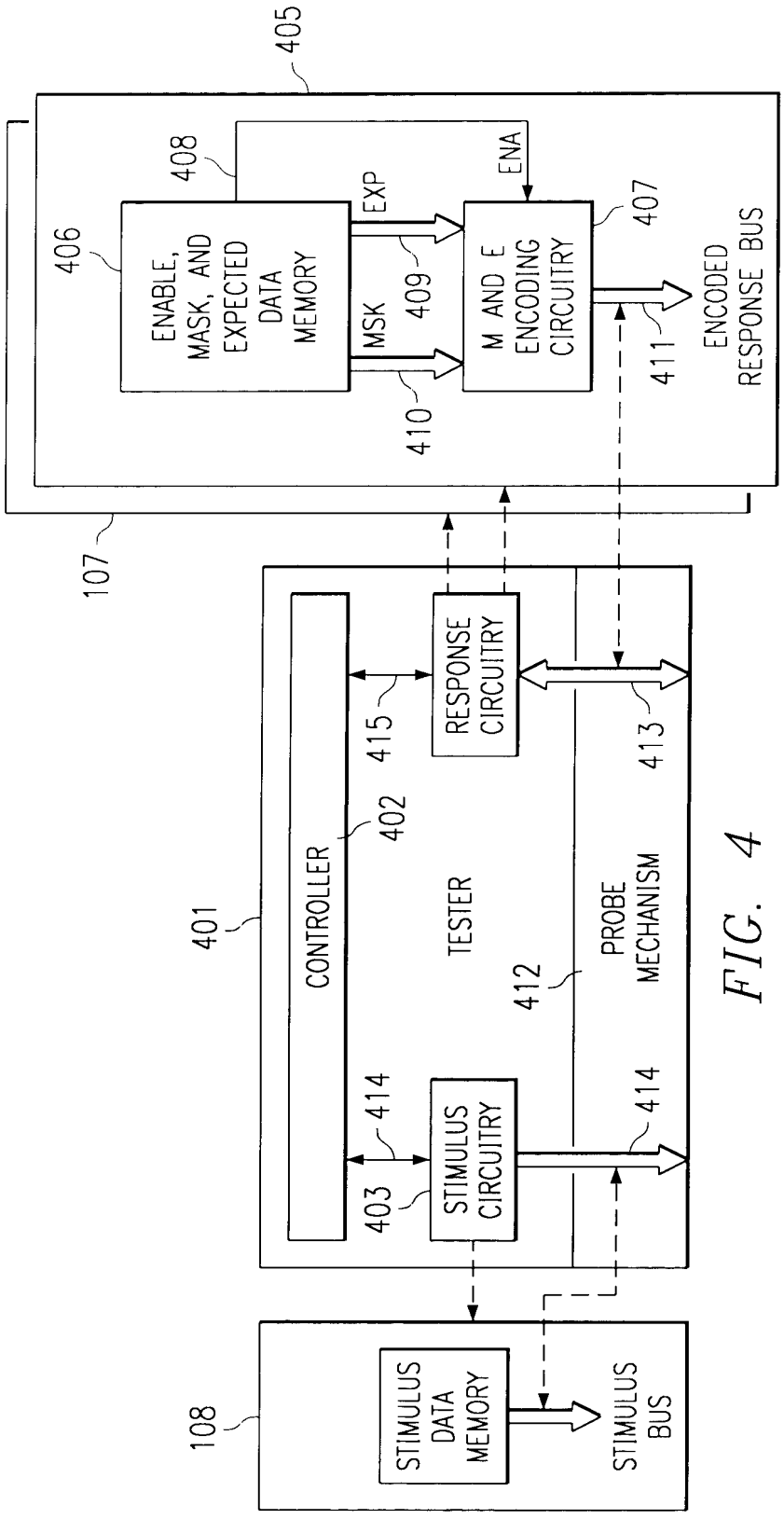

405
408
406
ENABLE, MASK, AND EXPECTED DATA MEMORY
EXP
ENA
407
MSK
409
M AND E ENCODING CIRCUITRY
410
411
ENCODED RESPONSE BUS
107
RESPONSE CIRCUITRY
415
413
401
CONTROLLER
402
TESTER
PROBE MECHANISM
412
414
414
STIMULUS CIRCUITRY
403
108
STIMULUS DATA MEMORY
STIMULUS BUS

FIG. 4

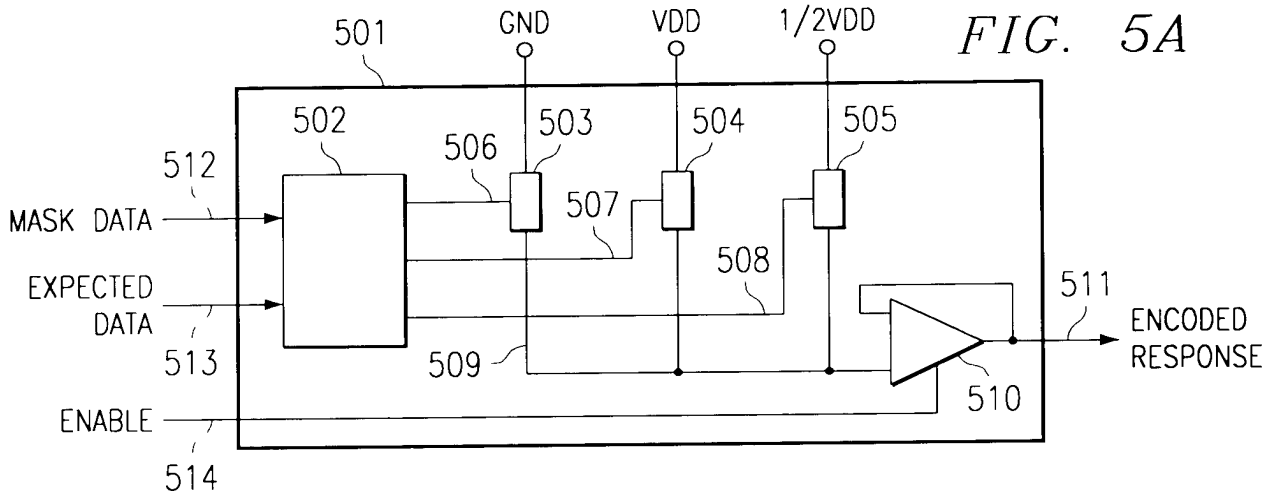


FIG. 5A

FIG. 5B

ENA	MSK	EXP	ENR	OUTPUT MODE
0	0	0	Z	DISABLED
1	0	0	GND	LOW
1	0	1	VDD	HIGH
1	1	X	1/2VDD	MASK

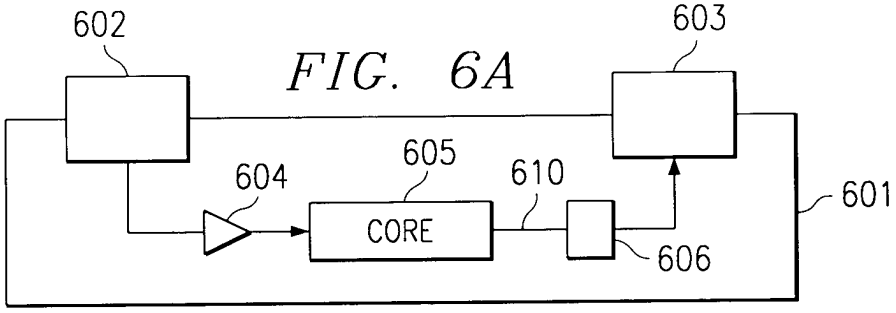


FIG. 6A

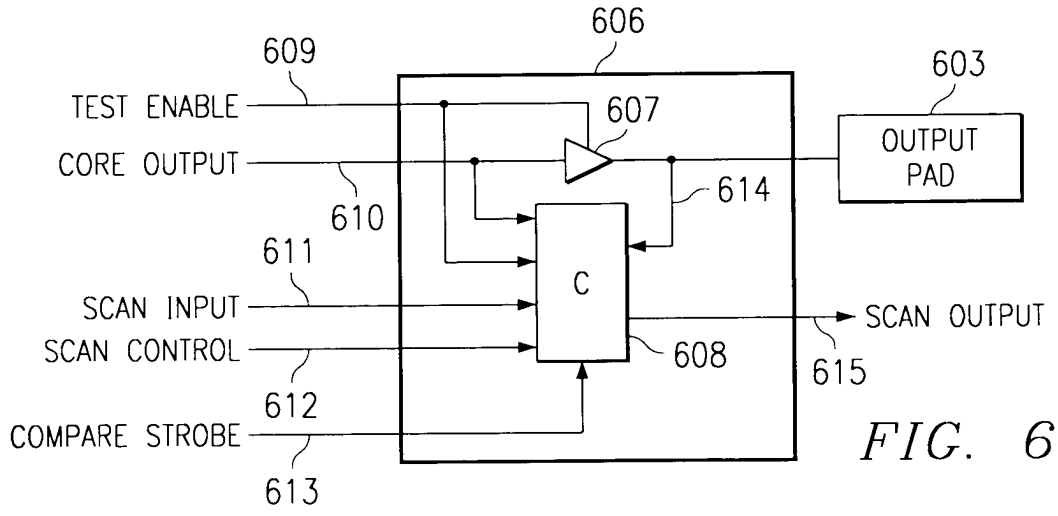


FIG. 6B

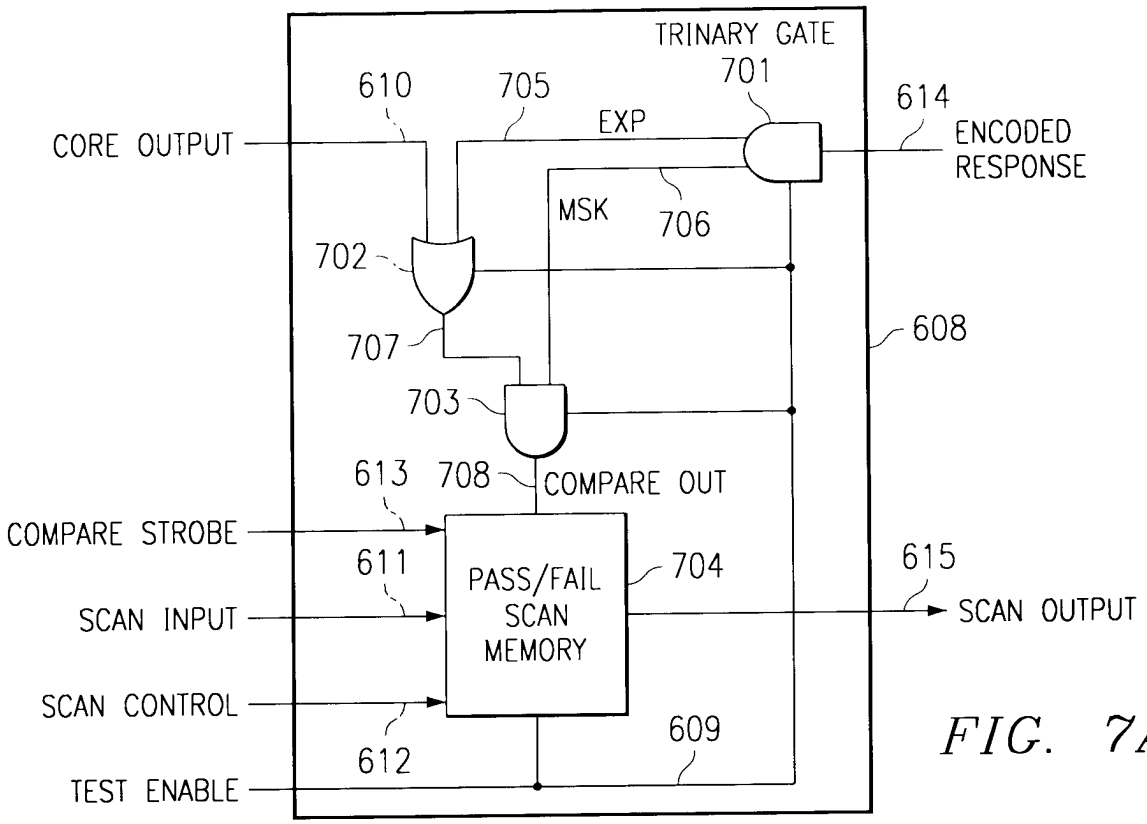


FIG. 7A

TEN	ENR	MSK	EXP	FUNCTION PERFORMED
0	X	X	X	TEST DISABLED
1	GND	1	0	COMPARE LOW
1	VDD	1	1	COMPARE HIGH
1	1/2VDD	0	X	MASK COMPARE

FIG. 7B

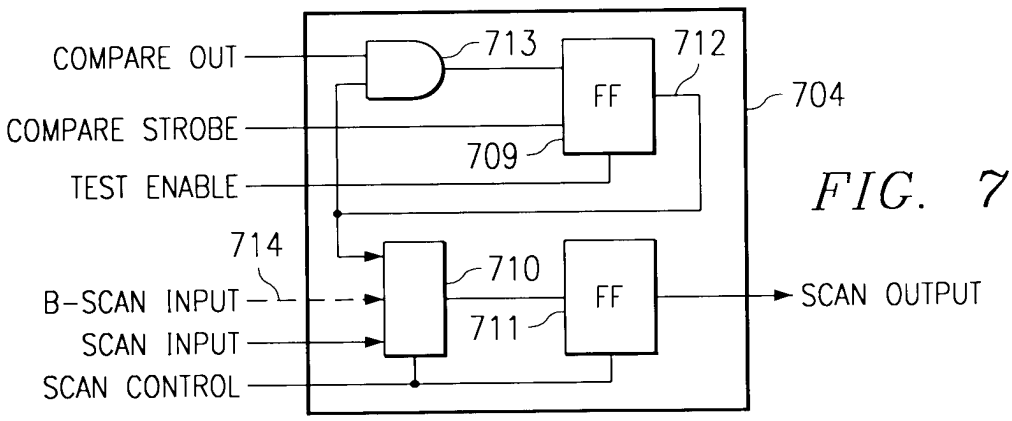


FIG. 7C

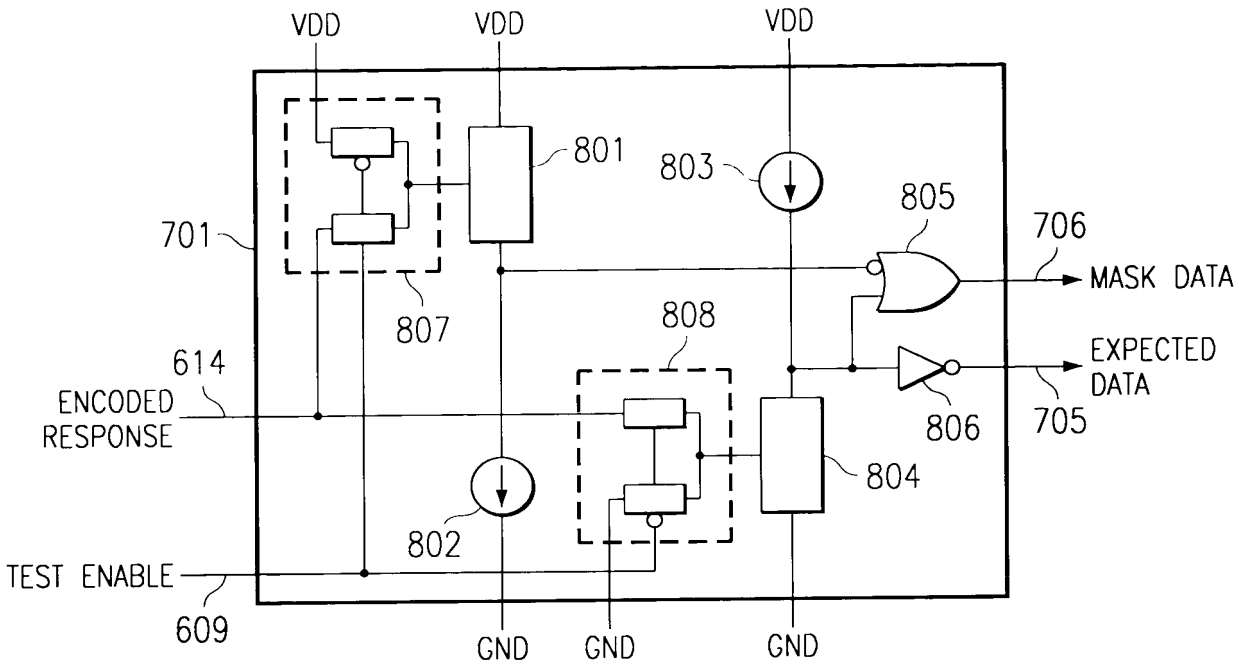


FIG. 8A

TEN	ENR	MSK	EXP	FUNCTION PERFORMED
0	X	1	0	GATE DISABLED
1	GND	1	0	OUTPUT A LOW
1	VDD	1	1	OUTPUT A HIGH
1	1/2VDD	0	X	OUTPUT A MASK

FIG. 8B

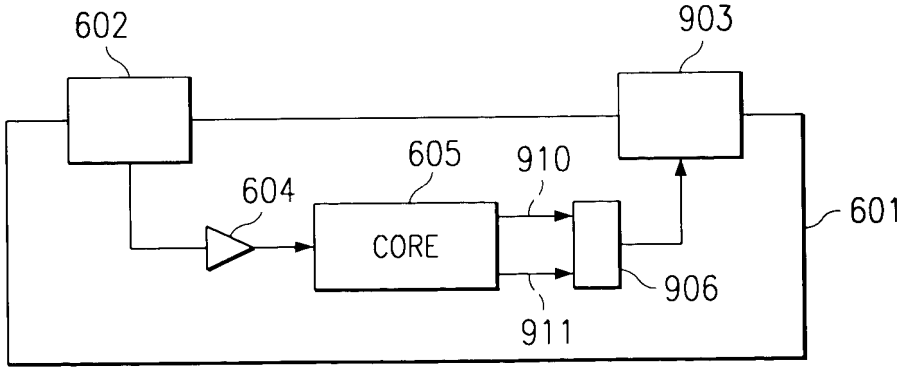


FIG. 9A

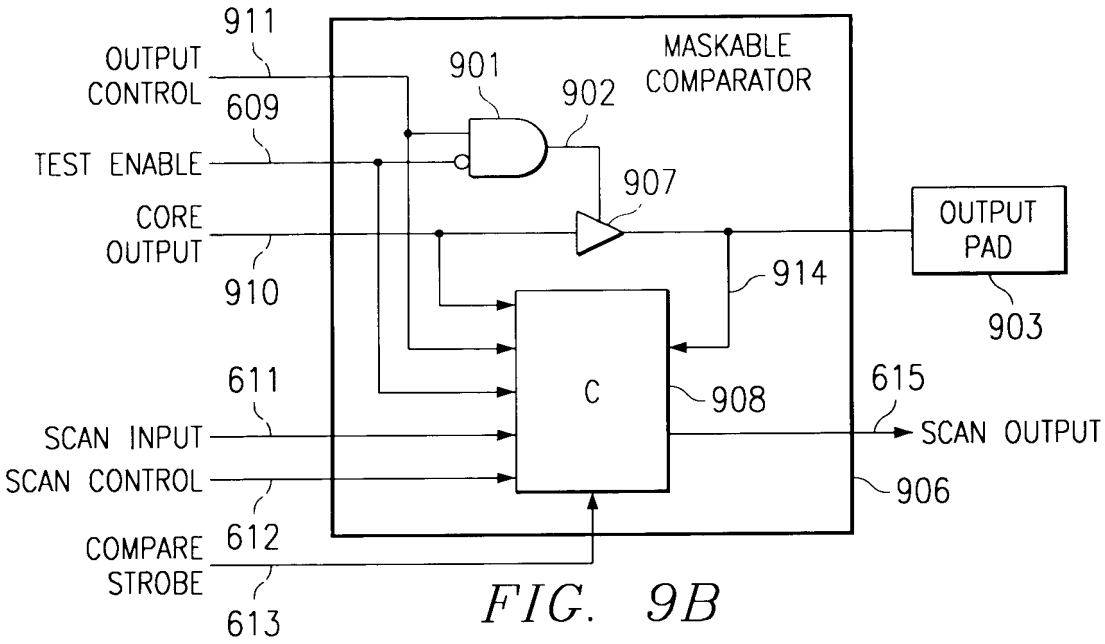


FIG. 9B

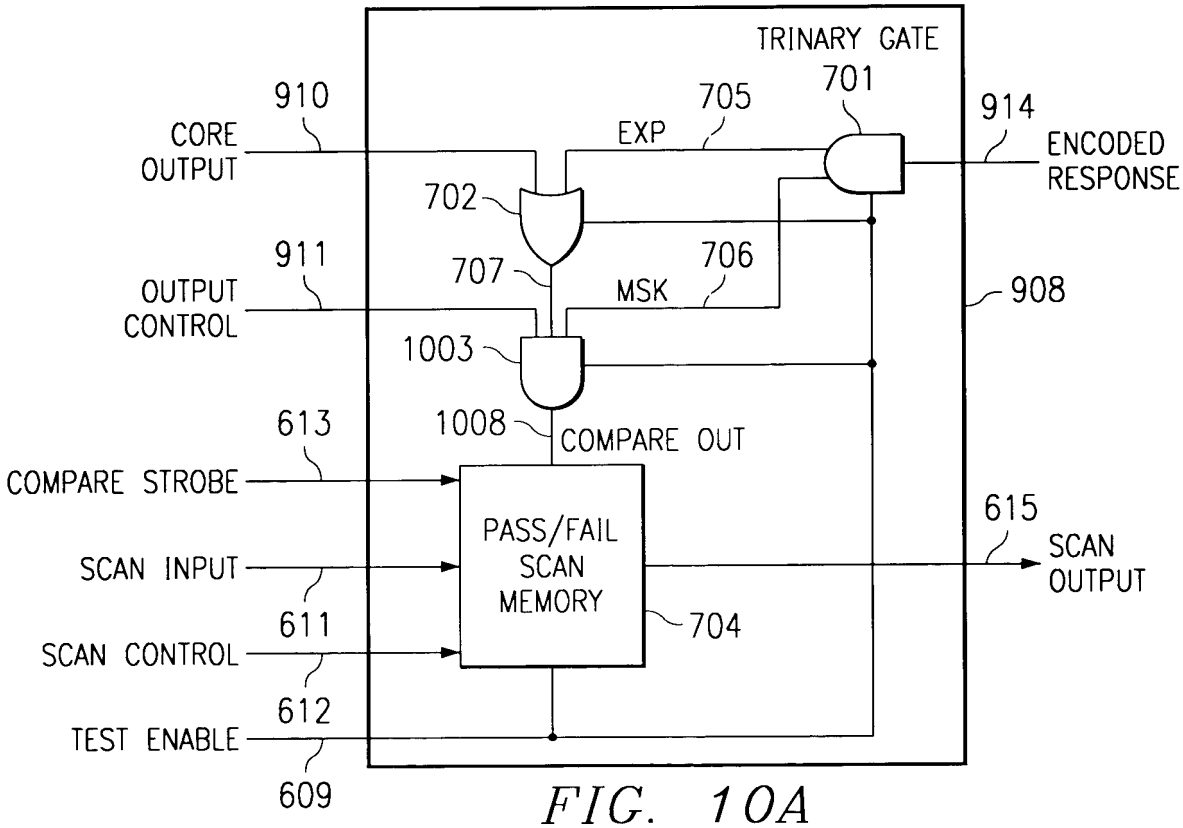


FIG. 10A

OC	TEN	ENR	MSK	EXP	FUNCTION PERFORMED
X	0	X	X	X	TEST DISABLED
1	1	GND	1	0	COMPARE LOW
1	1	VDD	1	1	COMPARE HIGH
1	1	1/2VDD	0	X	MASK COMPARE
0	1	GND/VDD	1	0/1	TEST OUTPUT CONTROL

FIG. 10B

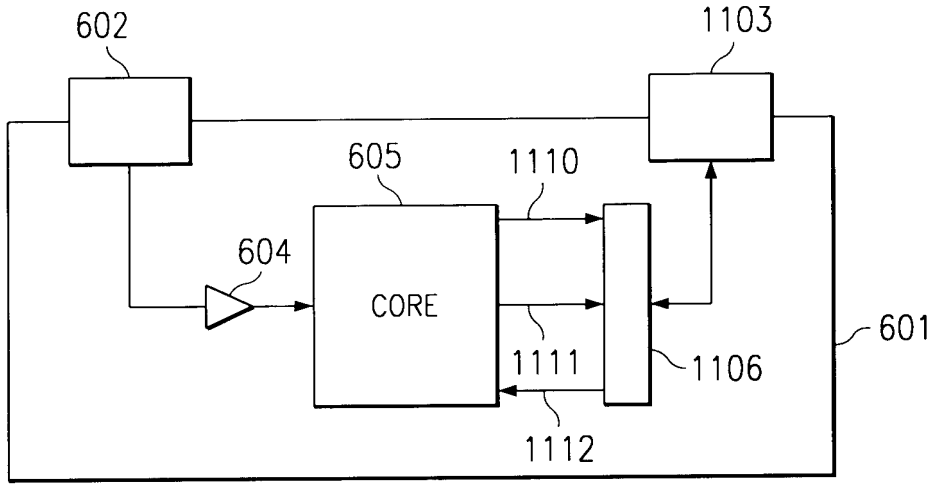


FIG. 11A

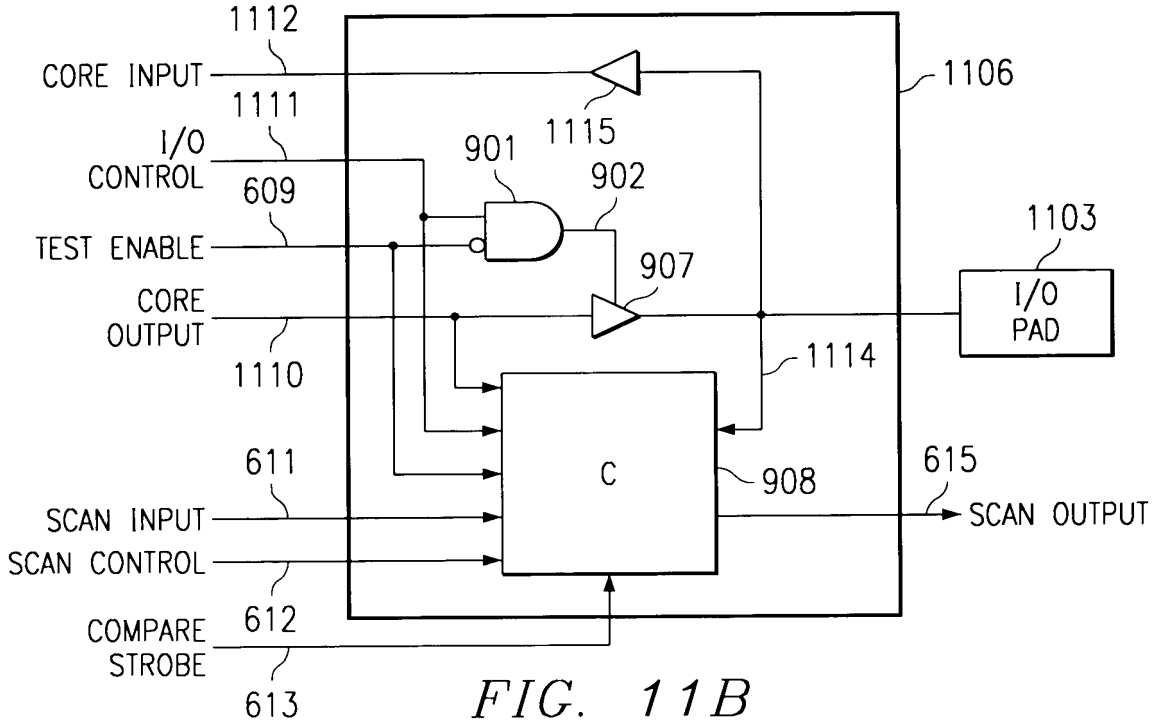


FIG. 11B

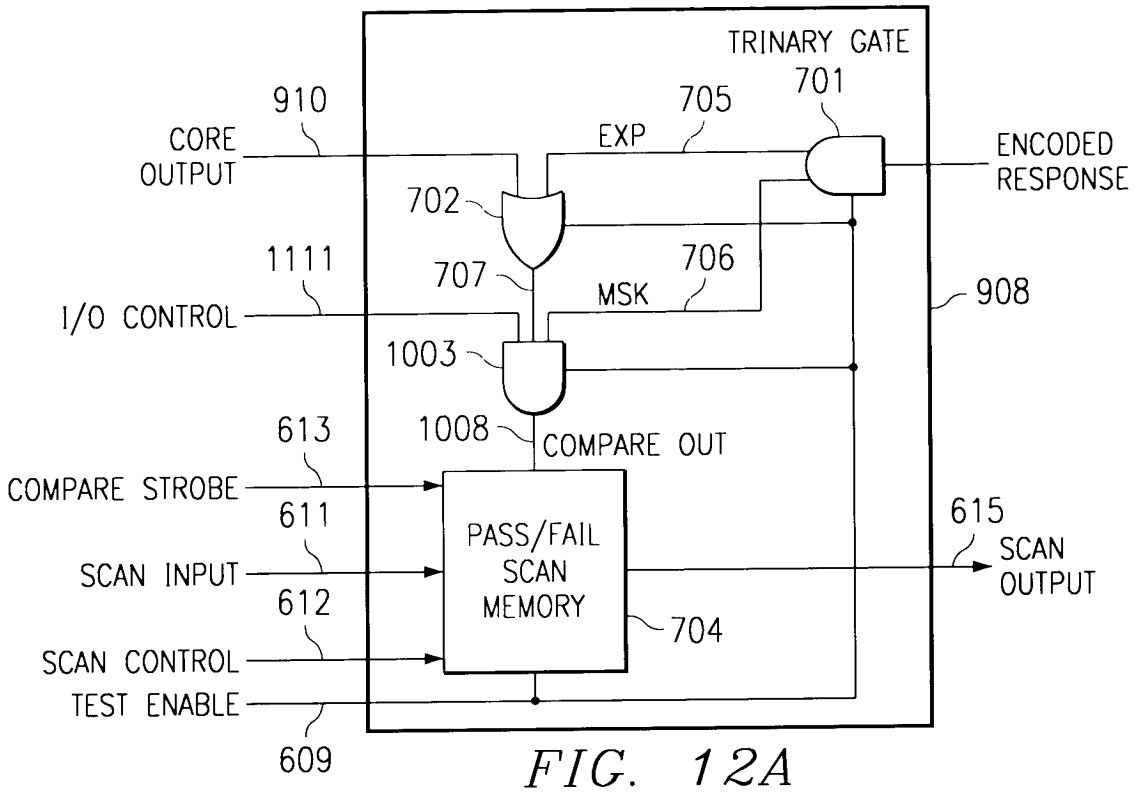


FIG. 12A

IOC	TEN	ENR	MSK	EXP	FUNCTION PERFORMED
X	0	X	X	X	TEST DISABLED
1	1	GND	1	0	COMPARE LOW
1	1	VDD	1	1	COMPARE HIGH
1	1	1/2VDD	0	X	MASK COMPARE
0	1	GND/VDD	1	0/1	TEST I/O CONTROL
0	1	GND/VDD	1	0/1	INPUT STIMULUS

FIG. 12B

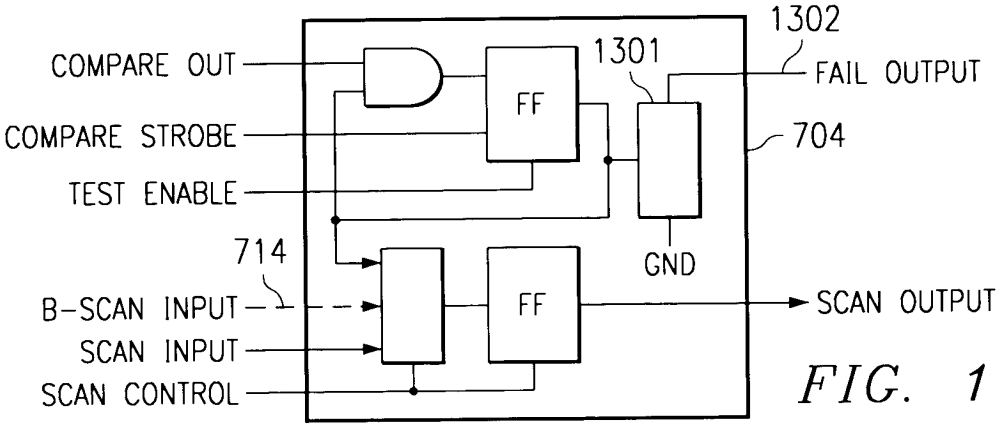


FIG. 13A

FIG. 13B

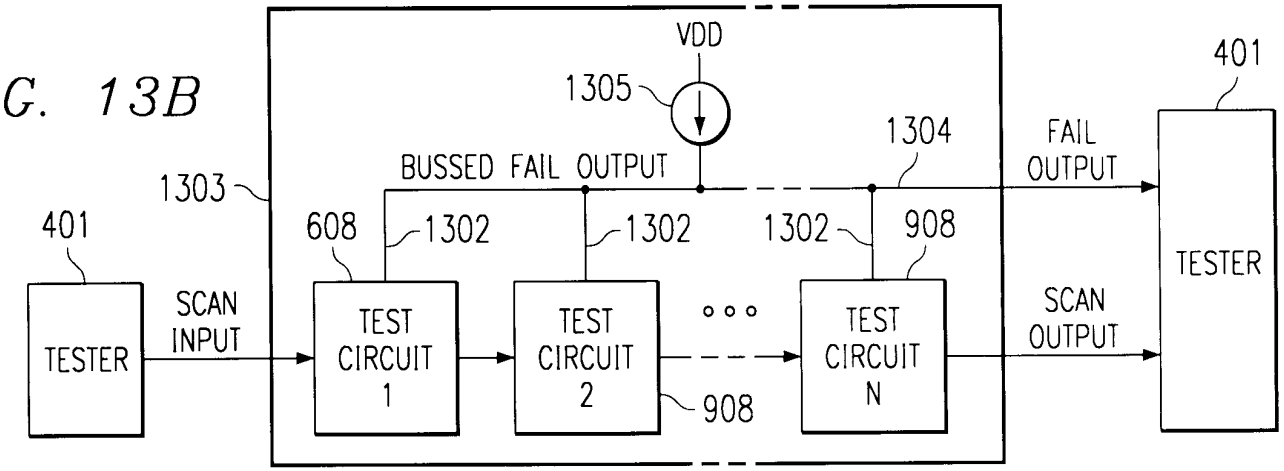


FIG. 14

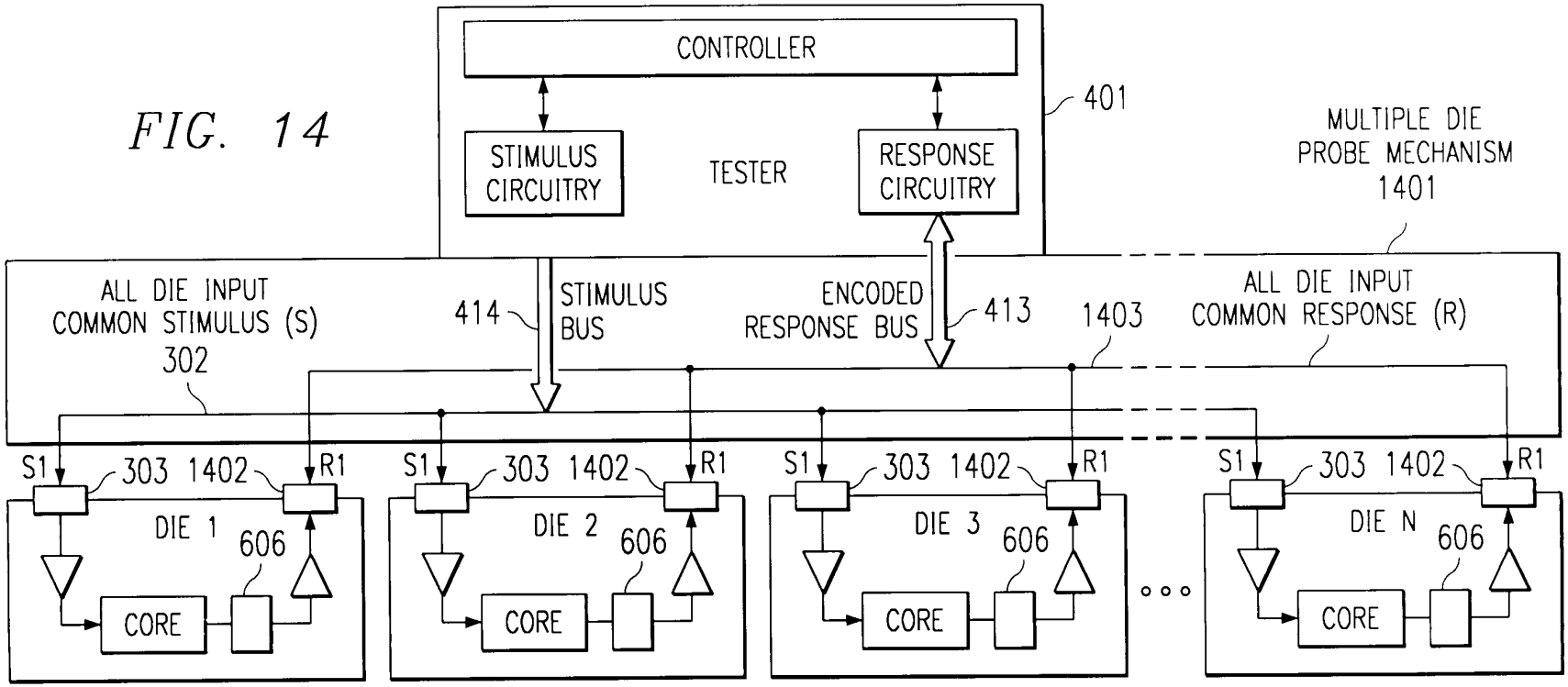
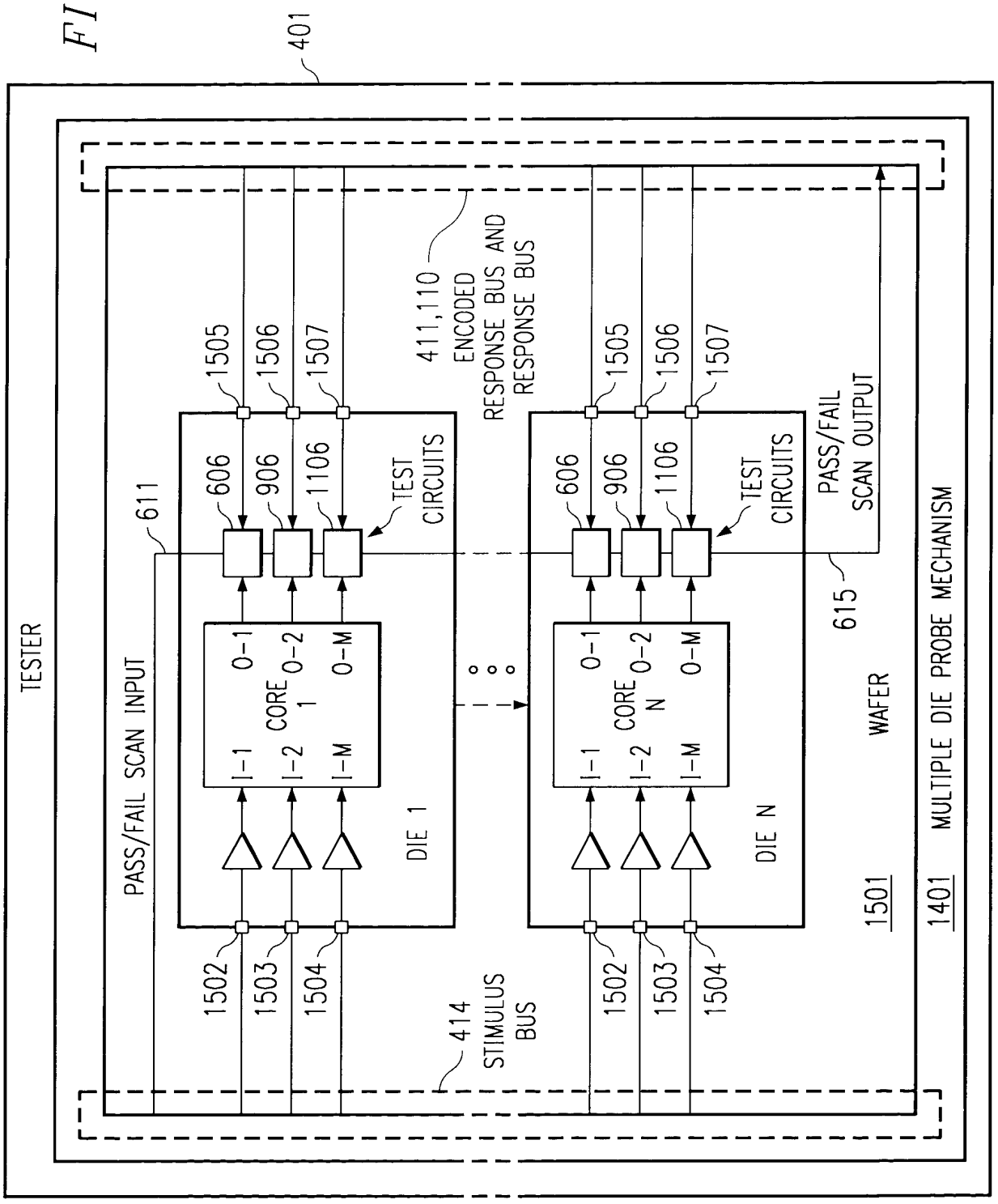


FIG. 15


401
TESTER
PASS/FAIL SCAN INPUT
611
1505
1506
1507
606
906
1106
TEST CIRCUITS
411,110
ENCODED RESPONSE BUS AND RESPONSE BUS
CORE 1
I-1
I-2
I-M
O-1
O-2
O-M
DIE 1
DIE N
CORE N
1502
1503
1504
414
STIMULUS BUS
615
PASS/FAIL SCAN OUTPUT
WAFER
1501
1401 MULTIPLE DIE PROBE MECHANISM

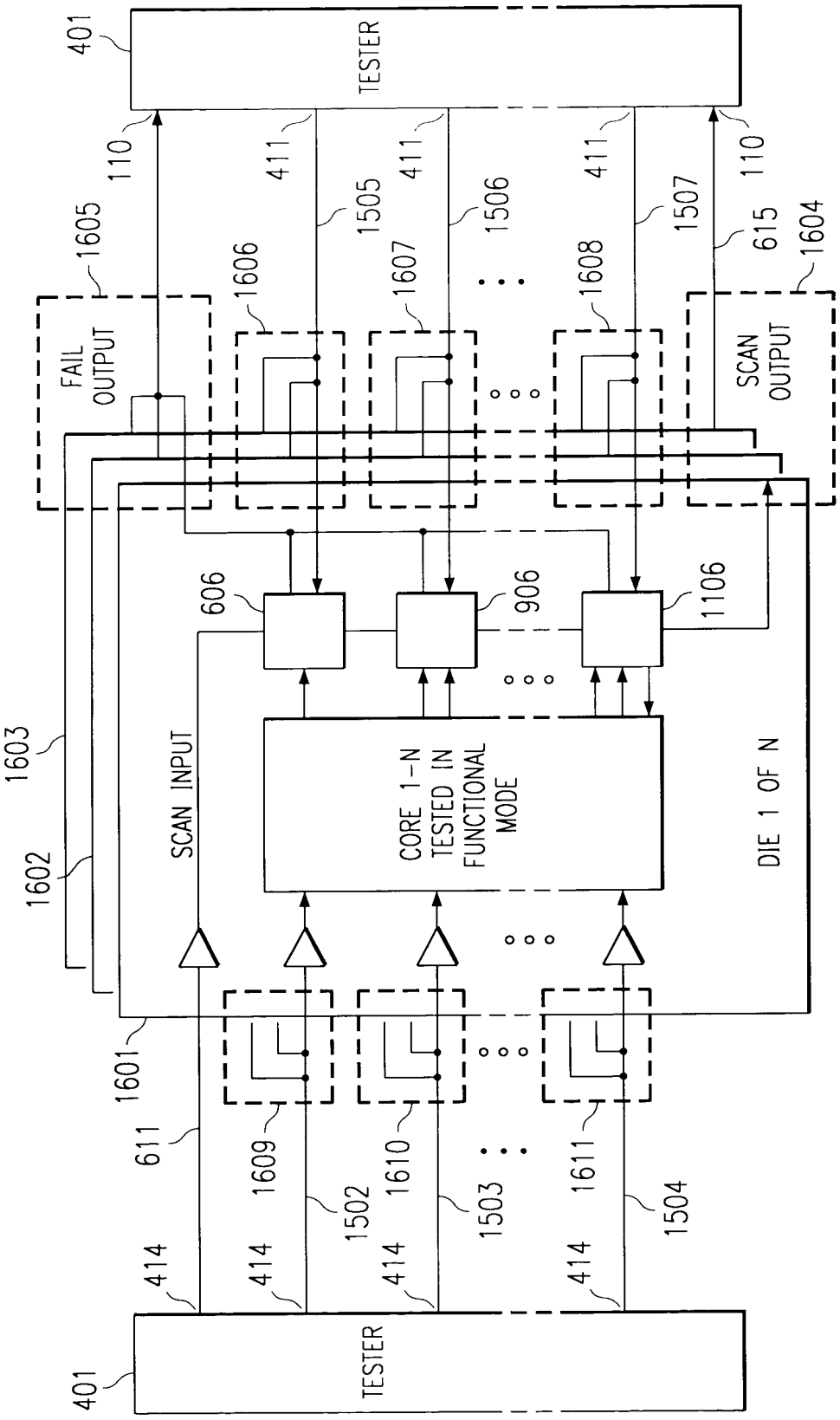

401
TESTER
110
411
1505
411
1506
411
1507
110
1605
1606
1607
1608
615
1604
FAIL OUTPUT
SCAN OUTPUT
606
906
1106
1603
1602
SCAN INPUT
CORE 1-N TESTED IN FUNCTIONAL MODE
DIE 1 OF N
1601
611
1609
1610
1611
1502
1503
1504
414
414
414
414
401
TESTER

FIG. 16

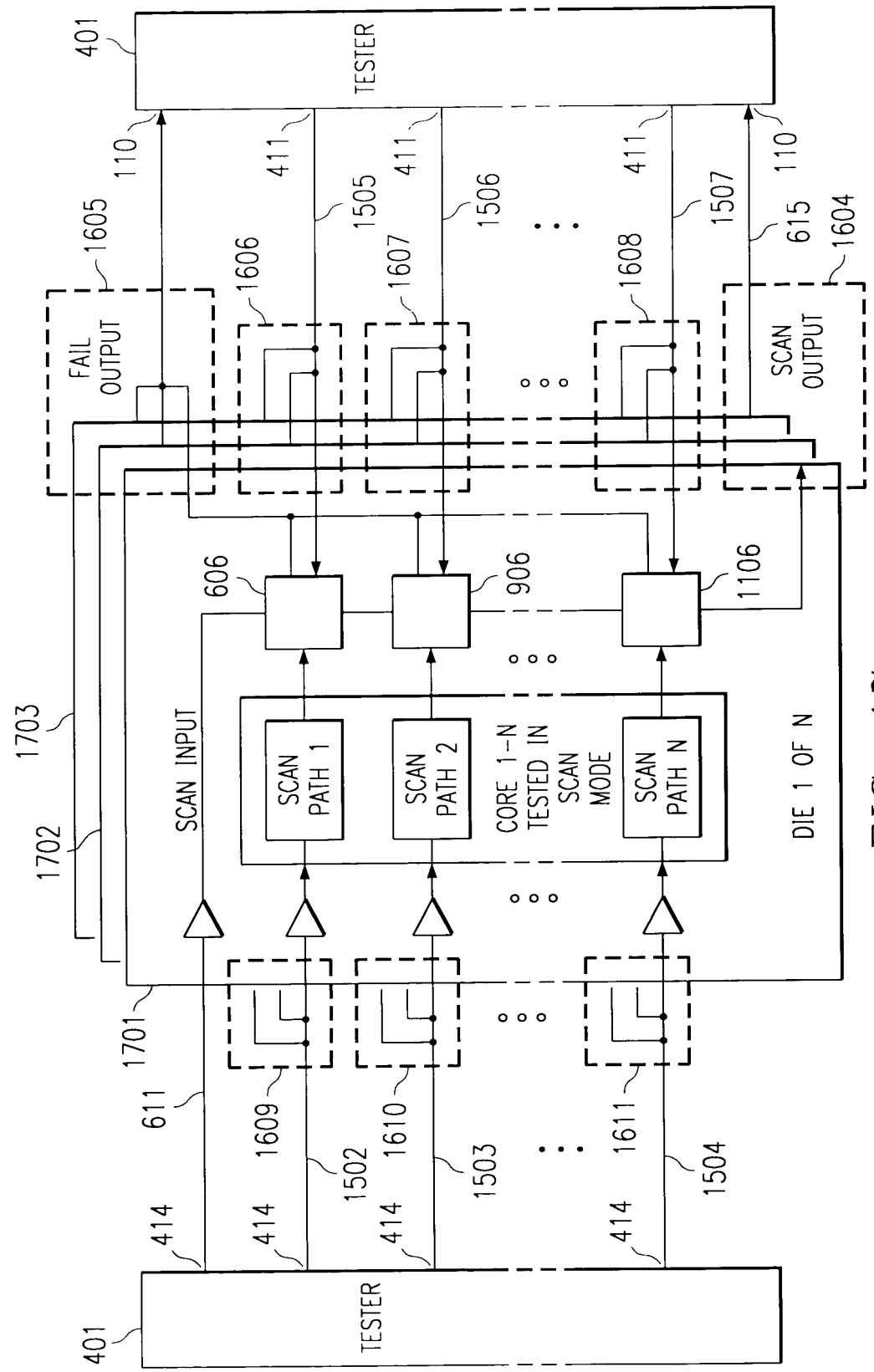

401
TESTER
110
411
1505
411
1506
411
1507
110
1605
1606
1607
1608
615
1604
FAIL OUTPUT
SCAN OUTPUT
606
906
1106
1703
SCAN INPUT
SCAN PATH 1
SCAN PATH 2
CORE 1-N TESTED IN SCAN MODE
SCAN PATH N
DIE 1 OF N
1702
1701
611
1609
1610
1611
1502
1503
1504
414
414
414
414
401
TESTER

FIG. 17

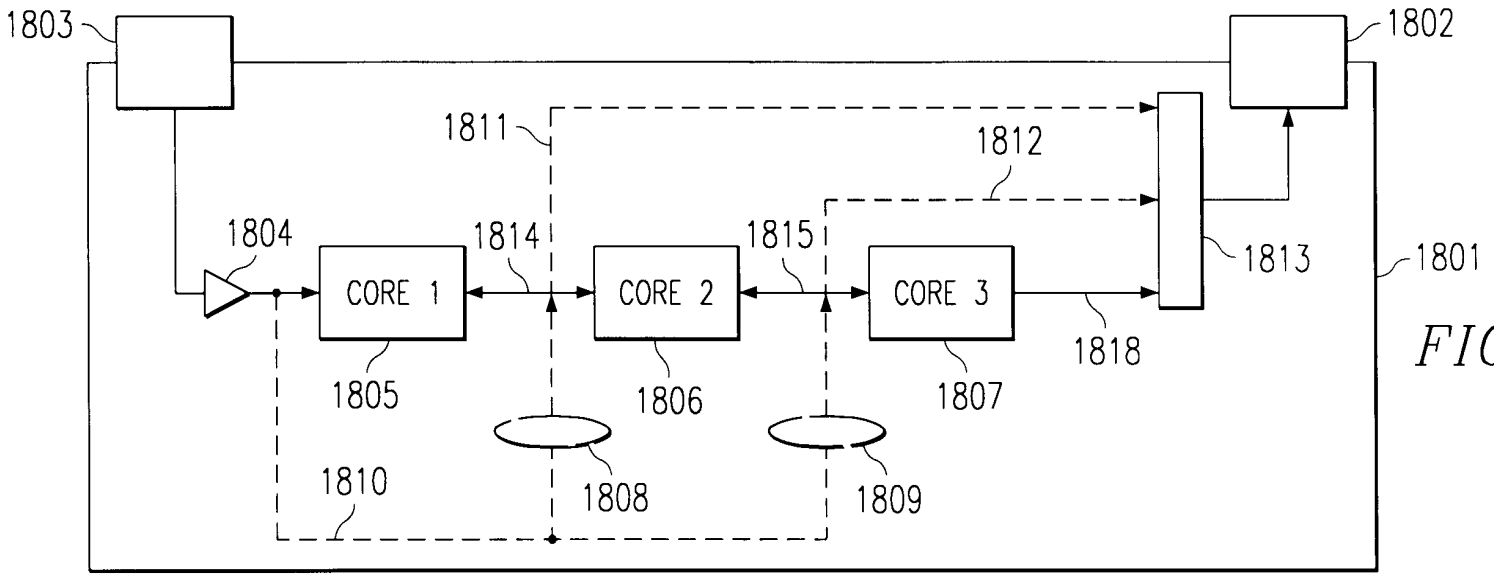


FIG. 18A

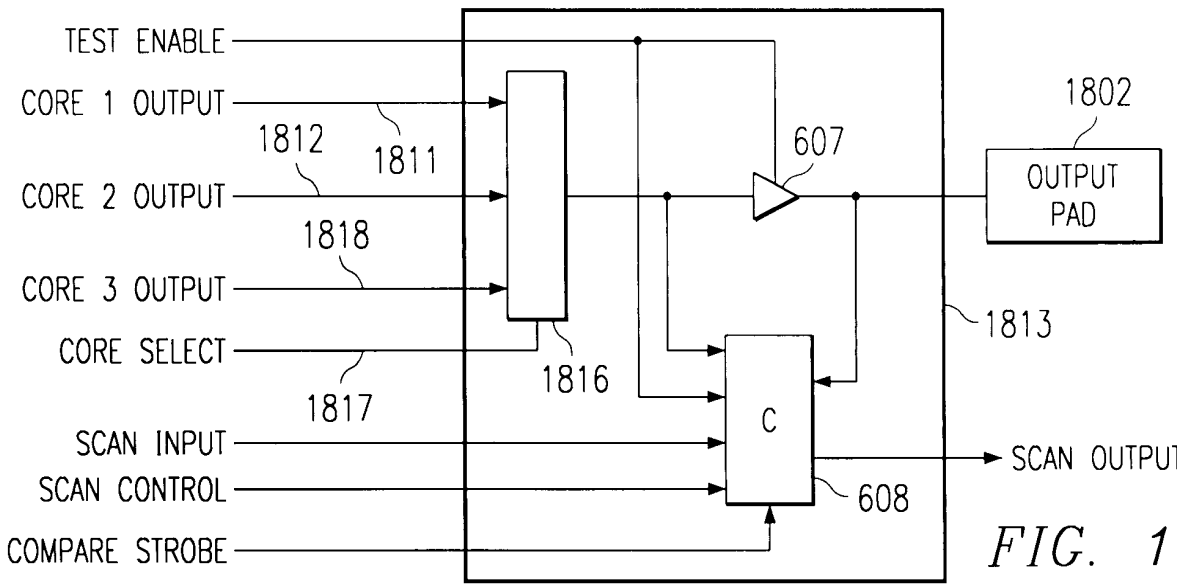


FIG. 18B

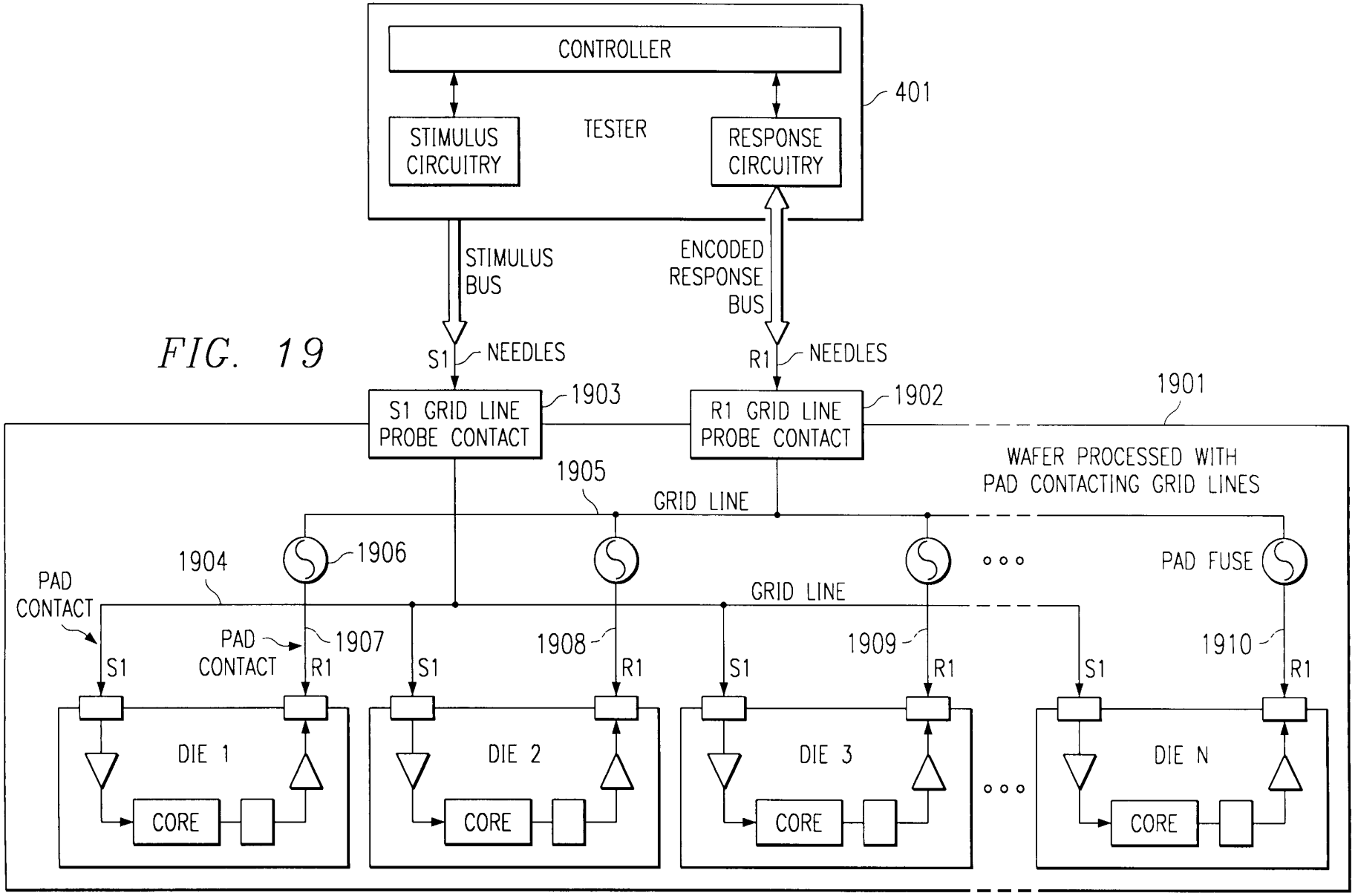
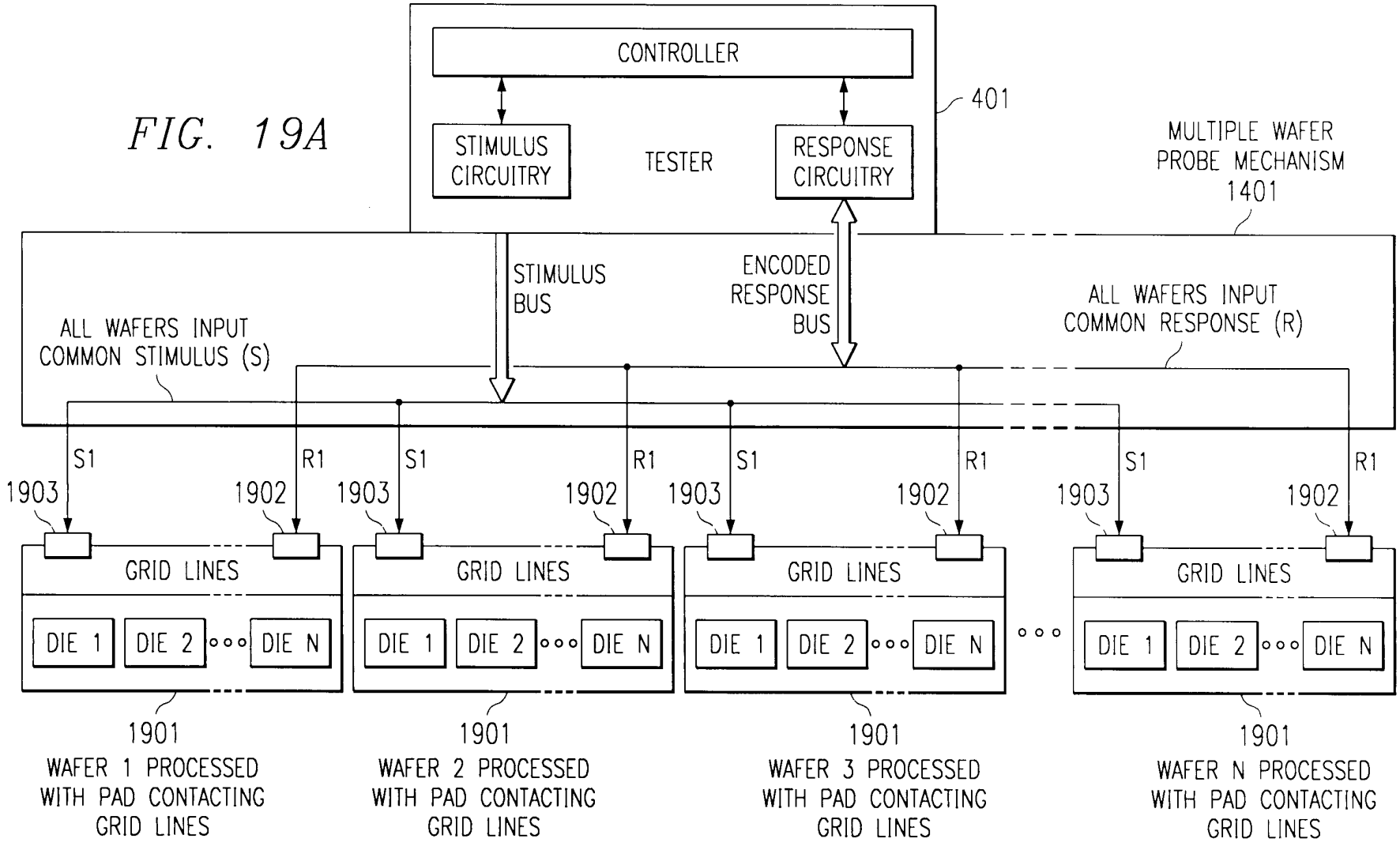

CONTROLLER
401
STIMULUS CIRCUITRY
TESTER
RESPONSE CIRCUITRY
STIMULUS BUS
ENCODED RESPONSE BUS
S1
NEEDLES
R1
NEEDLES
1901
S1 GRID LINE PROBE CONTACT
1903
R1 GRID LINE PROBE CONTACT
1902
WAFER PROCESSED WITH PAD CONTACTING GRID LINES
1905
GRID LINE
1904
1906
PAD FUSE
PAD CONTACT
GRID LINE
PAD CONTACT
1907
1908
1909
1910
S1
R1
S1
R1
S1
R1
S1
R1
DIE 1
DIE 2
DIE 3
DIE N
CORE
CORE
CORE
CORE

FIG. 19

FIG. 19A


CONTROLLER
401
STIMULUS CIRCUITRY
TESTER
RESPONSE CIRCUITRY
MULTIPLE WAFER PROBE MECHANISM 1401
STIMULUS BUS
ENCODED RESPONSE BUS
ALL WAFERS INPUT COMMON STIMULUS (S)
ALL WAFERS INPUT COMMON RESPONSE (R)
S1
R1
1903
1902
GRID LINES
DIE 1
DIE 2
DIE N
1901
WAFER 1 PROCESSED WITH PAD CONTACTING GRID LINES
WAFER 2 PROCESSED WITH PAD CONTACTING GRID LINES
WAFER 3 PROCESSED WITH PAD CONTACTING GRID LINES
WAFER N PROCESSED WITH PAD CONTACTING GRID LINES

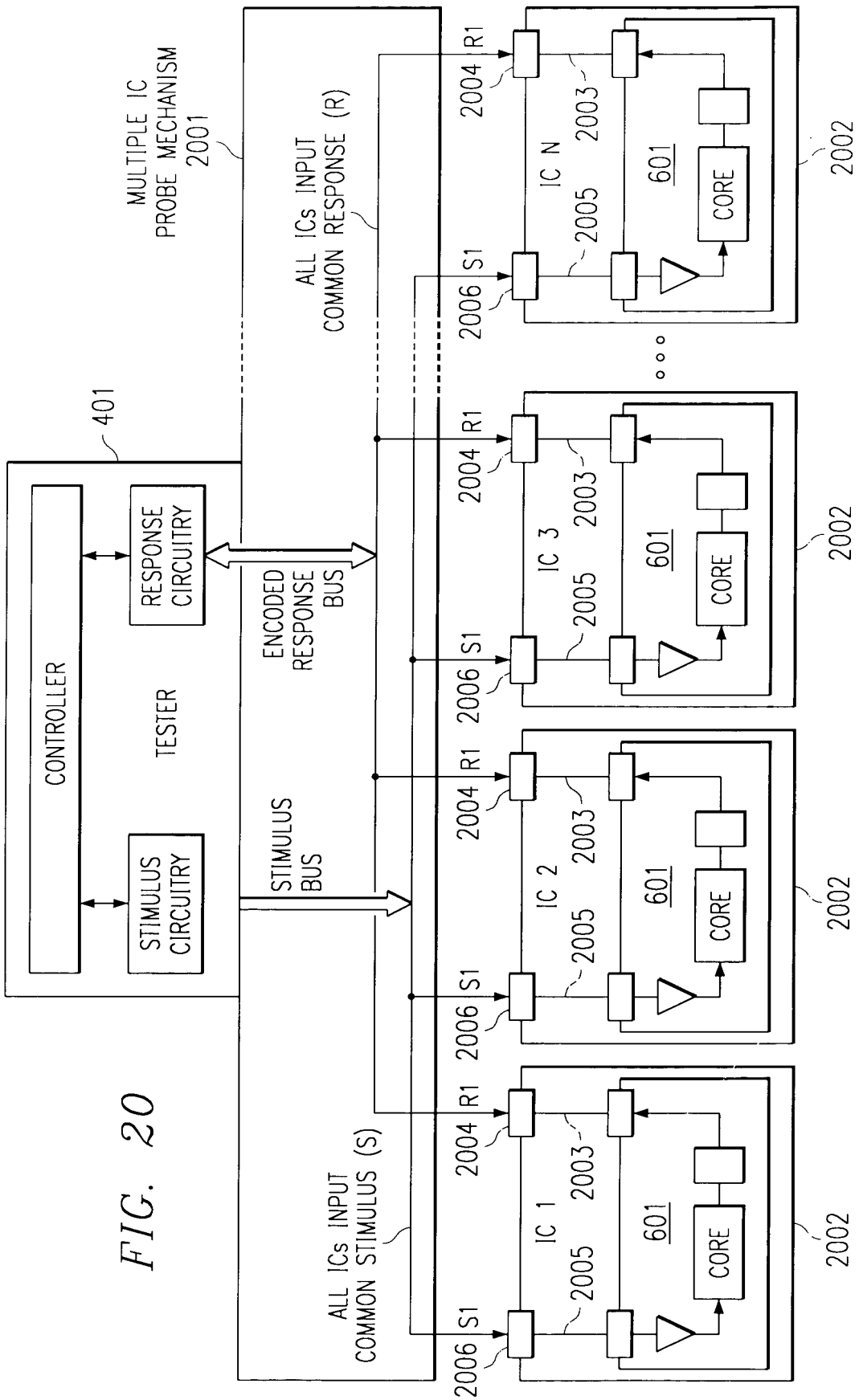

MULTIPLE IC
PROBE MECHANISM
2001
401
CONTROLLER
TESTER
RESPONSE
CIRCUITRY
STIMULUS
CIRCUITRY
ENCODED
RESPONSE
BUS
STIMULUS
BUS
ALL ICs INPUT
COMMON RESPONSE (R)
ALL ICs INPUT
COMMON STIMULUS (S)
IC 1
IC 2
IC 3
IC N
CORE
601
2002
2003
2004
2005
2006
R1
S1

FIG. 20